IN THE CLAIMS:

1. (Currently Amended) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a strained surface layer on a surface of said substrate by implanting ions of at least one heavy inert material through said surface of said substrate; ~~and~~

forming at least one gate structure above said strained surface layer; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the at least one field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

2. (Original) The method of claim 1, wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof, are implanted.

3. (Original) The method of claim 1, wherein the implanting energy is selected in the range of approximately 10-100 keV.

4. (Original) The method of claim 1, wherein the implanting dose is selected in the range of approximately $10^{13}/cm^2 - 10^{16}/cm^2$.

5. (Currently Amended) The method of claim 1, ~~wherein a thermal budget in manufacturing the field effect transistor is adjusted to substantially avoid grid restoration of the~~

~~substrate~~ wherein, prior to forming said strained surface layer, a gate insulation layer for said at least one field effect transistor is formed on a surface of said substrate and said step of implanting ions of at least one heavy inert material is performed through said gate insulation layer.

6. (Original) The method of claim 1, wherein said substrate comprises one of silicon and germanium or a combination thereof.

7. (Original) The method of claim 1, wherein said field effect transistor is one of an NMOS, a PMOS and a CMOS transistor.

8. (Currently Amended) A method of forming at least one field effect transistor on a semiconductive substrate, the method comprising

forming an insulating film on a surface of said substrate;

generating a strained surface layer at the interface of said insulating film and said substrate by implanting ions comprised of at least one heavy inert material through the ~~gate~~ insulating film into said substrate; ~~and~~

removing said insulating film;

forming a gate insulating ~~structure.~~ layer for said at least one field effect transistor on said surface of said substrate after said insulating film has been removed; and

performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the at least one field effect transistor

is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

9. (Original) The method of claim 8, wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof are implanted.

10. (Original) The method of claim 8, wherein the implanting energy is in the range of approximately 20-200 keV.

11. (Original) The method of claim 8, wherein the implanting dose is in the range of approximately $10^{13}/cm^2 - 10^{16}/cm^2$.

12. (Currently Amended) The method of claim 8, wherein ~~a thermal budget is adjusted to substantially avoid the grid restoration of said substrate~~ said strained surface layer has a thickness less than 20 nm.

13. (Original) The method of claim 8, wherein said substrate comprises one of silicon and germanium or a combination thereof.

14. (Original) The method of claim 8, wherein said field effect transistor is one of an NMOS, a PMOS and a CMOS transistor.

15. (Currently Amended) The method of claim 8, wherein said insulating film comprises oxide~~, the method further comprising patterning said insulating film to form said gate insulating film and forming a gate polysilicon structure on said gate insulating film~~.

16. (Currently Amended) The method of claim 8, ~~further comprising removing said insulating film after generating said strained layer, forming a gate insulating layer and patterning said gate insulating layer to form said insulating gate structure~~ wherein said gate insulating layer comprises silicon dioxide.

17. (New) The method of claim 1, wherein said strained surface layer has a thickness less than 20 nm.

18. (New) A method of forming at least one field effect transistor on a substrate, the method comprising:

forming a gate insulation layer for said at least one field effect transistor on a surface of said substrate;

forming a strained surface layer on a surface of said substrate by implanting ions of at least one heavy inert material through said gate insulation layer and into said substrate; and

forming at least one gate electrode structure above said gate insulation layer after forming said strained surface layer.

19. (New) The method of claim 18, wherein ions of at least one of xenon, argon, germanium, silicon, or a combination thereof, are implanted.

20. (New) The method of claim 19, further comprising performing additional process steps to manufacture said at least one field effect transistor, wherein a thermal budget in manufacturing the field effect transistor is adjusted to substantially avoid silicon grid restoration in the strained surface layer.

21. (New) The method of claim 19, wherein said strained surface layer has a thickness less than 20 nm.